

Pulsed Low Bias Frequencies for High Aspect Ratio Plasma Etching

Evan Litch¹, Hyunjae Lee³, Sang Ki Nam³ and Mark J. Kushner²

¹Nuclear Engr. & Radiological Sci., University of Michigan, Ann Arbor, Michigan, USA

²Electrical Engr. & Computer Sci., University of Michigan, Ann Arbor, Michigan, USA

³Mechatronics Research, Samsung Electronics Co., Ltd., Republic of Korea

elitch@umich.edu, hj0928.lee@samsung.com, sangki.j.nam@samsung.com, mjkush@umich.edu

Current roadmaps for microelectronics fabrication are focused on fabrication of 3-dimensional devices for higher functionality. Plasma etching steps during fabrication of these 3D devices are becoming increasingly more challenging due to the high aspect ratios (HARs) of the features [1]. For example, 3D-NAND memory structures contain hundreds of alternating layers of SiO₂ and Si₃N₄ requiring etching of vias having aspect ratios (AR) exceeding 100. Deep trench isolation (DTI) for electrical isolation of the 3D logic structures have similar HAR challenges. DTI etching of conductive substrates such as Si using halogen gas mixtures (e.g. HBr/Cl₂) is typically performed in inductively coupled plasmas (ICPs) with a substrate bias to facilitate highly anisotropic etching.

Plasma etching of HAR features requires ion energy and angular distributions (IEADs) that are narrow in angle while extending to energies exceeding several kV. These requirements motivate the use of very low frequency biases (VLF) – a few hundred kHz. Trends in the industry are also moving towards pulsed biases to optimize the ratio of radical to ion fluxes. Several challenges arise with the use of pulsed, low frequency, high voltage biases. The thickening of the sheath and charging of focus rings (structures surrounding the wafer) lead to edge exclusion – a region at the edge of the wafer where IEADs are perturbed from their desired, ideal anisotropic properties. These undesirable properties generally result from sheath curvature. The transient nature of pulsed biases exacerbate these challenges by introducing additional sheath curvature.

In this presentation, results will be discussed from a computational investigation of IEADs incident onto wafers and remediation of edge exclusion when using pulsed VLF biases in ICPs for etching of trenches for DTI. Simulations were conducted using the Hybrid Plasma Equipment Model (HPEM) [2]. Operating conditions are tens of mTorr mixtures of Ar/Cl₂/O₂ with bias frequencies from 250 kHz to 5 MHz. Bias voltages are up to a few kV with pulse repetition frequencies of up to several kHz. The consequences of these operating conditions on etching DTI features were evaluated using the Monte

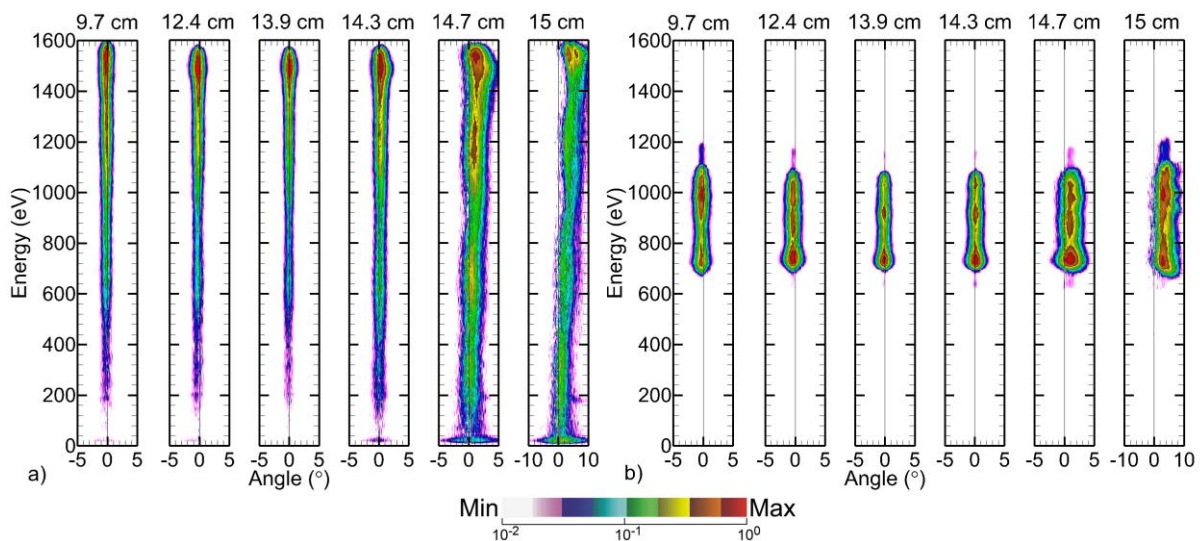


Fig. 1. Ion energy and angular distributions (IEADs) at radial positions approaching the wafer edge for (left) 250 kHz and (right) 5 MHz.

Carlo Feature Profile Model (MCFPM) [2]. When using continuous wave biases, the charging of the focus ring is sensitive to frequency, and this charging produces sheath curvature at the edge of the wafer, which perturbs IEADs. For example, IEADs are shown in Fig. 1 approaching the edge of a 30 cm diameter wafer for bias frequencies of 250 kHz and 5 MHz for an ICP sustained in Ar/Cl₂/O₂ with bias voltage amplitude of 1 kV. With pulsed biasing, the focus ring is transiently charged both during the VLF cycle and during the pulsed cycle, adding additional challenges to minimizing edge exclusion.

This work was supported by Samsung Electronics Co. and the US National Science Foundation (2009219).

- [1] J. Kim, G. Choi, and K.-H. Kwon, *Plasma Processes Polym.* **20**, e2200167 (2023).
- [2] S. Huang, et al., *J. Vac. Sci. Technol. A* **37**, 031304 (2019).